Amendment to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims

Claims 1-6 (canceled)

Claim 7 (currently amended): A semiconductor memory comprising:

a memory cell having ferroelectric capacitor which is selectively connected to a first bit line through a switching device;

a sense amplifier for comparing an electric potential of said first bit line with a reference potential in order to read out data in said memory cell when said memory cell is connected to said first bit line through said switching device;

first and second dummy memory cells having ferroelectric capacitors which ~~can be~~ are selectively connected to a second bit line and a third bit line through switching devices in order to apply said reference potential to said sense amplifier; and

short-circuit means which short-circuits said second and third bit lines at the time of said data reading,

wherein said ferroelectric capacitors of both of said dummy memory cells are polarized to opposite directions relative to one another, and

wherein, when the data is read out, the operation to apply the electric potentials from both of said dummy memory cells to each bit line corresponding thereto is executed in a state where both of said second and third bit lines are mutually electrically shut off, and thereafter, an intermediate value of both electric potentials of both of said second and third bit lines which is obtained by said short-circuit of both of said second and third bit lines by said short-circuit means is supplied as [[a]] the reference potential to said sense amplifier.

Claim 8 (previously presented): A memory according to claim 7, wherein the polarizing directions of said ferroelectric capacitors of both of said dummy memory cells are sequentially reversed to opposite directions every said data reading.

Claim 9 (previously presented): A semiconductor memory comprising:

a memory cell having ferroelectric capacitor which is selectively connected to a first bit line through a switching device;

a sense amplifier for comparing an electric potential of said first bit line with a reference potential in order to read out data in said memory cell when said memory cell is connected to said first bit line through said switching device;

first and second dummy memory cells having ferroelectric capacitors which ~~can be~~ are selectively connected to a second bit line and a third bit line through switching devices in order to apply said reference potential to said sense amplifier; and

short-circuit means which short-circuits said second and third bit lines at the time of said data reading,

wherein said ferroelectric capacitors of both of said dummy memory cells are polarized to opposite directions relative to one another, and

wherein each time the data is read out, the polarizing directions of said ferroelectric capacitors of both of said dummy memory cells are sequentially reversed to opposite directions.

Claim 10 (original): A memory according to claim 9, wherein an intermediate value of both electric potentials of said bit lines which are applied from said ferroelectric capacitors of both of said dummy memory cells to each of said bit lines corresponding thereto is supplied as a reference potential to said sense amplifier.

Claim 11 (original): A memory according to claim 9, wherein the operation to

apply the electric potentials from both of said dummy memory cells to each bit line corresponding thereto is executed in a state where both of said second and third bit lines are mutually electrically shut off, and thereafter, an intermediate value of both electric potentials of both of said second and third bit lines which is obtained by the short-circuit of both of said second and third bit lines by said short-circuit means is supplied as a reference potential to said sense amplifier.

12. (previously presented): A semiconductor memory, comprising:

first, second and third bit lines:

a first memory cell which induces a first electric potential onto the first bit line;

a first dummy memory cell having a ferroelectric capacitor polarized to a first direction and inducing a second electric potential onto the second bit line;

a second dummy memory cell having a ferroelectric capacitor polarized to a second direction opposite to said first direction and inducing a third electric potential onto the third bit line;

a short-circuiting device which electrically shorts said second and third bit lines;

a sense amplifier which compares an electric potential of said first bit line with an electric potential of said second bit line and outputs an amplified voltage to each of said first and second bit lines in accordance with a result of said comparison.

13. (previously presented): The method according to claim 12, wherein the first bit line is one of a plurality of bit lines located in a first area of the semiconductor memory, and the second and third bit lines are two of a plurality of bit lines located in a second area of the semiconductor memory.

14. (previously presented): The method according to claim 13, further comprising a second memory cell which induces a fourth electric potential onto a fourth bit line.

15. (previously presented): The method according to claim 14, further comprising a third dummy memory cell having a ferroelectric capacitor polarized to the first direction and inducing a fifth electric potential onto a fifth bit line.

16. (previously presented): The method according to claim 15, further comprising a fourth dummy memory cell having a ferroelectric capacitor polarized to a second direction opposite to said first direction and inducing a sixth electric potential onto a sixth bit line.

17. (previously presented): The method according to claim 16, further comprising a second short-circuiting device which electrically shorts said fifth and sixth bit lines.

18. (previously presented): The method according to claim 17, further comprising a second sense amplifier which compares an electric potential of said fourth bit line with an electric potential of said fifth bit line and outputs an amplified voltage to each of said fourth and fifth bit lines in accordance with a result of said comparison.